	Туре	Hits	Search Text	DBs
1	BRS	333	712/218.ccls.	USPAT
2	BRS	383	712/216.ccls.	USPAT
3	BRS	572	713/600.ccls.	USPAT ,
4	BRS	846	(reorder or retirement) adj buffer	USPAT
5	BRS	853	(reorder or retirement) adj (buffer or array)	USPAT
6	BRS	729	((reorder or retirement) adj (buffer or array)) and clock	USPAT
7	BRS	347	((reorder or retirement) adj (buffer or array)) same clock	USPAT
8	BRS	1097	((reorder\$3 or (re-order\$3) or (re adj order\$3)) or retir\$6) adj (buffer or array)	USPAT
9	BRS	898	((reorder\$3 or (re-order\$3) or (re adj order\$3)) or retir\$6) adj (buffer or array) and clock\$3	USPAT
10	BRS	387	((reorder\$3 or (re-order\$3) or (re adj order\$3)) or retir\$6) adj (buffer or array) same clock\$3	USPAT

BEST AVAILABLE COPY

08/17/2004, EAST Version: 1.4.1

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



TECE HOME I SEANC	HIEEE I SHOP I WEB ACCOUNT I CONTACT IEEE	ĒĿ
Membership Public	cations/Services Standards Conferences Careers/Jobs	
	Welcome United States Patent and Trademark Office	1 1
Help FAQ Terms IE	EEE Peer Review Quick Links >>	Se
Welcome to IEEE Xplore		
O- Home O- What Can I Access? O- Log-out	Your search matched 10 of 1062489 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevan Descending order.	106
Tables of Contents	Refine This Search:	
O- Journals & Magazines	You may refine your search by editing the current search expression or entinew one in the text box. ((retirement <in>ti) <or></or></in>	eri
Conference Proceedings	Check to search within this result set	
O- Standards	Results Key:	
«Search [®] de la	JNL = Journal or Magazine CNF = Conference STD = Standard	
O- By Author	•	
O- Basic	1 Complexity-effective reorder buffer designs for superscalar proces	SS
O- Advanced	Kucuk, G.; Ponomarev, D.V.; Ergin, O.; Ghose, K.;	
MidderSandes	Computers, IEEE Transactions on , Volume: 53 , Issue: 6 , June 2004 Pages:653 - 665	
O- Join IEEE	[Abstract] [PDF Full-Text (1376 KB)] IEEE JNL	
Web Account	2 A novel reordering write buffer to improve write performance of lo	— იc
O- Access the IEEE Member	structured file systems Jun Wang; Yiming Hu;	-2
Digital Library	Computers, IEEE Transactions on , Volume: 52 , Issue: 12 , Dec. 2003	
THE Enterprise	Pages:1559 - 1572	
O- Access the	[Abstract] [PDF Full-Text (2135 KR)] TEEF 184	

O Access the IEEE Enterprise File Cabinet

Print Format

[Abstract] [PDF Full-Text (2135 KB)] IEEE JNL

3 Checkpoint processing and recovery: an efficient, scalable alternative reorder buffers

Akkary, H.; Rajwar, R.; Srinivasan, S.T.;

Micro, IEEE, Volume: 23, Issue: 6, Nov.-Dec. 2003

Pages:11 - 19

[Abstract] [PDF Full-Text (244 KB)] IEEE JNL

4 Distributed reorder buffer schemes for low power

Kucuk, G.; Ergin, O.; Ponomarev, D.; Ghose, K.;

Computer Design, 2003. Proceedings. 21st International Conference on , 13-

Oct. 2003

Pages:364 - 370

[Abstract] [PDF Full-Text (267 KB)] IEEE CNF

5 Context reorder buffer: an architectural support for real-time proce on RISC architectures

Caironi, P.V.C.; Mezzalira, L.; Sami, M.;

Real-Time Systems, 1996., Proceedings of the Eighth Euromicro Workshop or 14 June 1996

Pages: 262 - 270

[Abstract] [PDF Full-Text (920 KB)]

6 A 56-entry instruction reorder buffer

Gaddis, N.B.; Butler, J.R.; Kumar, A.; Queen, W.J.; Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSC(1996 IEEE International, 8-10 Feb. 1996 Pages: 212 - 213, 447

[PDF Full-Text (1068 KB)] **IEEE CNF** [Abstract]

7 Reducing reorder buffer complexity through selective operand cach

Kucuk, G.; Ponomarev, D.T.; Ergin, O.; Ghose, K.; Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 200. International Symposium on , 25-27 Aug. 2003

Pages: 235 - 240

[PDF Full-Text (783 KB)] [Abstract] **IEEE CNF**

8 Using rewriting rules and positive equality to formally verify wide-is out-of-order microprocessors with a reorder buffer

Velev, M.N.;

Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings , 4-8 March 2002

Pages:28 - 35

[PDF Full-Text (253 KB)] [Abstract] **IEEE CNF**

9 Design and implementation of a 100 MHz reorder buffer

Wallace, S.; Dagli, N.; Bagherzadeh, N.;

Circuits and Systems, 1994., Proceedings of the 37th Midwest Symposium

on , Volume: 1 , 3-5 Aug. 1994

Pages: 42 - 45 vol. 1

[PDF Full-Text (292 KB)] [Abstract] **IEEE CNF**

10 On the reduction of reorder buffer size for discrete Fourier transfol processor design

Wen-Zen Shen; Yi-Hsin Tao; Lan-Rong Dung;

Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on , Volume: 4 , 30 May-2 June 1994

Pages: 171 - 174 vol.4

[PDF Full-Text (368 KB)] **IEEE CNF** [Abstract]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online

Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

BEST AVAILABLE COPY